

1 **IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

2 Application Serial No. 10/826,228
3 Filing Date May 16, 2004
4 Inventor Hogdal, G.
5 Group Art Unit..... 2113
6 Examiner C. McCarthy
7 Applicant..... Microsoft Corporation
8 Attorney's Docket No. MS1-671USC1
9 Title: Systems and Methods for Replicating Virtual Memory On A Host Computer
10 and Debugging Using Replicated Memory
11
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13 **RESPONSE TO FINAL OFFICE ACTION DATED APRIL 28, 2006**

14 To: To: Mail Stop AF
15 Commissioner for Patents
16 PO Box 1450
17 Alexandria, VA 22313-1450
18
19 From: Mark C. Farrell Reg. No. 45,988
20 (Tel. 509-324-9256x216; Fax 509-323-8979)
21 Lee & Hayes, PLLC
22 421 W. Riverside Ave., Suite 500
23 Spokane, WA 99201
24
25

Customer # 22801

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INTRODUCTORY COMMENTS

The Applicant appreciates the Patent Office's previous finding of allowable subject matter. This Amendment is in Response to a final Office Action of April 28, 2006. Applicant suggests that the amendments herein should put this application in condition for allowance.

Amendments to the Claims begins on page 3 of this paper.

A Listing of the Claims begins on page 4 of this paper.

Remarks begin on page 9 of this paper.

Listing of the Claims

1. (Currently Amended) A method for debugging a target computer that utilizes virtual memory paging, the method comprising:

replicating on a host computer an address translation table of the target computer, wherein the address translation table establishes on the host computer correspondences between physical memory addresses and virtual memory addresses that existed on the target computer;

transferring physical memory data from the target computer to the [[a]] host computer; and

replicating virtual memory data from the physical memory data on the host computer, wherein the virtual memory data on the host computer is identical to virtual memory data on the target computer.

2. (Original) The method as recited in claim 1, further comprising debugging a fault on the target computer by analyzing replicated data on the host computer.

3. (Original) The method as recited in claim 1, further comprising caching the replicated data in memory on the host computer.

4. (Original) The method as recited in claim 1, wherein the target computer includes an operating system that uses table-driven paged memory management.

1 5. (Previously Presented) The method as recited in claim 1,
2 wherein:

3 the target computer includes a processor that has halted execution; and
4 the virtual memory data is located in physical memory of the target
5 computer.

6
7 6. (Currently Amended) A host computing system, comprising:
8 a processor;
9 memory;
10 means for establishing a connection between the memory and memory of a
11 target computer;

12 a data retrieval component configured to transfer address table data from
13 memory of the target computer to the memory;

14 an address translation component configured to replicate virtual memory
15 addresses from the address table data in the memory; and

16 wherein the virtual memory data in the host computing system are identical
17 to virtual memory data of the target computer for debugging the target computer
18 when a CPU of the target computer is halted.

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20 7. (Original) The host computing system as recited in claim 6,
21 further comprising cache memory configured to store the replicated virtual
22 memory addresses.
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1 8. (Original) The host computing system as recited in claim 6,
2 wherein the host-side address translation component is further configured to
3 validate the replicated virtual memory addresses.

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5 9. (Original) The host computing system as recited in claim 6,
6 further comprising a memory management verifier that verifies that a processor of
7 the target computing system has memory management enabled.

8
9 10. (Original) The host computing system as recited in claim 6,
10 wherein the means for establishing a connection between the memory and memory
11 of a target computer comprises hardware-assisted debug probes.

12
13 11. (Currently Amended) A method, comprising:
14 accessing address tables from physical memory of a target computer system
15 by reading the target memory directly through an application program interface;
16 replicating the address tables on a host computing system; and
17 using data contained in the address tables to derive virtual address data that
18 was used on the target computer system, wherein the virtual address data on the
19 host computer system are identical to virtual address data on the target computer
20 system.

21
22 12. (Original) The method as recited in claim 11, further comprising
23 storing the address tables in memory on the host computer system.

1 13. (Original) The method as recited in claim 11, further comprising
2 caching the virtual address data on the host computer system.

3
4 14. (Canceled)

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6 15. (Original) The method as recited in claim 11, further comprising
7 determining if memory management of a target computer system processor is
8 enabled.

9
10 16. (Original) The method as recited in claim 11, further comprising
11 performing the method only if memory management of a target computer system
12 processor is enabled.

13
14 17. (Original) The method as recited in claim 11, wherein the
15 accessing further comprises:

16 locating the address tables in physical memory of the target computer
17 system; and

18 reading the address tables from the target computer.

19
20 18. (Original) The method as recited in claim 11, further comprising
21 validating the virtual address data to ensure it is identical to the virtual address data
22 stored on the target computer system.

1 19. (Original) The method as recited in claim 11, further comprising
2 debugging a fault that occurred on the target computer by analyzing the virtual
3 address data on the host computer system.
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5 20. (Original) A computer-readable medium containing processor-
6 executable instructions that, when executed on a processor, perform the method of
7 claim 11.
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9 21-25. (Canceled)
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1 **REMARKS**

2 Claims 1-13, 15-25 were previously pending.

3 Please amend claims 1, 6, and 11.

4 Claim 14 is previously canceled.

5 Please cancel claims 21-25.

6 No new claims are added.

7 Claims 1-13, 15-20 are currently pending.

8
9 Applicant respectfully requests reconsideration and allowance of the subject
10 application.

11
12 **1. Double Patenting**

13 Claims 1-13, 15-25 were rejected on the ground of nonstatutory
14 obviousness-type double patenting over claims of U.S. Patent No. 6,766,472.
15 Claims 21-25 are canceled. Base claims 1, 6, and 11 are amended. Applicant
16 submits that the currently pending claims, after amendment, do not double patent
17 the same invention as the claims of U.S. Patent No. 6,766,472. Applicant
18 respectfully requests that the rejection be removed.

19
20 **2. Statutory 35 USC 101 double patenting**

21 Claims 1-5 were provisionally rejected under 35 USC 101 as claiming the
22 same invention as US Patent Application No. 11/276,644. Applicant suggests that
23 the rejection is moot as base claim 1 has been amended. Claims 2-5 include the
24 language of base claim 1. Thus, Applicant respectfully requests that the rejection
25 be removed.

1
2 **3. Double Patenting**

3 Claims 6-10 were rejected on the ground of nonstatutory obviousness-type
4 double patenting over claims of U.S. Patent Application No. 11/276,644.
5 However, claim 6 has been amended. Applicant submits that claims 6-10 do not
6 double patent the same invention as the claims of U.S. Patent Application No.
7 11/276,644. Applicant respectfully requests that the rejection be removed.

8
9 Claims 1-13, 15-25 were rejected on the ground of nonstatutory
10 obviousness-type double patenting over claims 1-18 of U.S. Patent Application
11 No. 11/276,633. Claims 21-25 have been canceled.

12 Applicant respectfully disagrees that given a method claim, an apparatus or
13 module claim to practice the method claim is automatically obvious. However,
14 base claims 1, 6, and 11 have been amended, so Applicant suggests that the
15 rejection is moot. Applicant respectfully requests that the rejection be removed.

16
17 **4. Patentable Distinction between Related Cases**

18 Regarding sections 7 and 9 of the Office Action, Applicant submits that the
19 claims of U.S. Patent Application No. 11/276,644 and the claims of U.S. Patent
20 Application No. 11/276,633 do not anticipate Applicant's claims because
21 Applicant's unamended claims were filed earlier in time than the claims of U.S.
22 Patent Application No. 11/276,644 and the claims of U.S. Patent Application No.
23 11/276,633. However, Applicant has amended all the current base claims to more
24 particularly point out and distinctly claim the subject matter.
25

1 **5. Duty to Disclose**

2 With regard to section 11 of the Office Action, Applicant suggests that
3 typically moving an element from the body of a claim to its preamble, or vice
4 versa, changes the scope of the claim (a preamble is not necessarily an element of
5 its claim). Therefore, Applicant did not intend that claims between related
6 applications should materially affect the patentability of each other and any
7 similarity that is deemed too close is merely an oversight. Thus, there was no duty
8 to disclose the later claims in the earlier application, even though Applicant
9 normally discloses all relationships between applications as a matter of standard
10 practice (see, for example, “related applications” heading and section at the
11 beginning of Applicant’s specification).

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13 **6. Amendments to Base Claims 1, 6, and 11**

14 Applicant amends the base claims to more particularly point out the subject
15 matter. Specifically, for example in claim 1, by replicating on a host computer an
16 address translation table of the target computer the host computer can replicate an
17 exact or similar condition of the virtual memory set up as it existed on the target
18 computer before the target computer’s CPU halted. This allows the target
19 computer to be debugged on a working host computer.

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22 **Conclusion**

23 Applicant suggests that all pending claims 1-13 and 15-20 are now in
24 condition for allowance. Applicant respectfully requests reconsideration and
25 issuance of the subject application. If any issues remain that prevent issuance of

1 this application, the Examiner is urged to contact the undersigned attorney before
2 issuing a subsequent Action.
3

4 Respectfully Submitted,
5

6 Date: 6/30/06
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By: /Mark C. Farrell/

8 Mark C. Farrell
9 Reg. No. 45,988
10 (509) 324-9256 x 243
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